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MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
BECK, ALEXANDER S	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/993,563	HAM, YONG SUNG	
	Examiner	Art Unit	
	Alexander S. Beck	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,15,16,18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,15,16,18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgment is made of the amendment filed by the Applicant on January 3, 2007, in which: Claims 1,2,4-6,8,9 and 11 are amended; and the rejections of the claims are traversed. Claims 1-11,15,16,18 and 20 are currently pending in U.S. Application Serial No. 09/993,563, and an Office Action on the merits follows.

Response to Arguments

2. Applicant's arguments with respect to Claims 1-11,15,16,18 and 20 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 5-8 and 18** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Independent **Claim 5** contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Specifically, the limitation "*a modulator to modulate the most significant bits of data of data including most significant bits of data and least significant bits of data*" is not supported by the specification of the instant application because there is no description as to how the data modulator modulates data including least

significant bit data. Rather, the specification of the instant application discloses and illustrates that the least significant bit data is not modulated. Only the most significant bit data is modulated.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-8,15,16 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission of Prior Art (hereinafter AAPA) in view of Hirosawa et al. (U.S. Patent No. 5,123,059, hereinafter HIROSAWA).

As to independent **Claim 1**, AAPA teaches/suggests a method of driving a liquid crystal display in **Figure 4**, comprising: dividing input data into most significant bit data and least significant bit data; delaying the most significant bit data for one frame period; and generating modulated current most significant bit data in accordance with a difference between the delayed most significant bit data and the current most significant bit data and independently from the least significant bit data (AAPA: pg. 7, par. [0012] – pg. 8, par. [0016]).

AAPA does not disclose expressly wherein the modulated current most significant bit data contains more data bits than do each of the current most significant bit data and the delayed most significant bit data.

As can be seen from **Figure 4** of AAPA, a look-up table receives input most significant bit data and outputs modulated most significant bit data. HIROSAWA, analogous in art with AAPA,

teaches/suggests a method of driving a liquid crystal display in **Figure 5** wherein input data of m-bits is received by a look-up table (**LUT**), the look-up table modulating the input data of m-bits by outputting modulated data of n-bits, wherein n is greater than m (n>m) (HIROSAWA: col. 5, ln. 20-30). This is accomplished by increasing the number of bits of the look-up table (HIROSAWA: col. 6, ln. 22-26).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of AAPA by increasing the number of bits of the look-up table such that the look-up table for receiving input data of m-bits outputs modulated data of n-bits, wherein n is greater than m, as taught/suggested by HIROSAWA. As a result, the modulated current most significant bit data containing more data bits than do each of the most significant bits of data of the delayed and current frame.

The suggestion/motivation for doing so would have been to improve the precision of the data to be displayed (HIROSAWA: col. 6, ln. 22-26).

As to independent **Claim 5**, AAPA teaches/suggests a driving apparatus for a liquid crystal display in **Figure 4**, comprising: a memory to receive most significant bits of data for an nth frame from an input line and to output the most significant bits of data for an $(n-1)^{th}$ frame; and a modulator to modulate the most significant bits of data including most significant bits of data and least significant bits of data of the n^{th} frame in accordance with a difference between the most significant bits of data for the $(n-1)^{th}$ frame and the most significant bits of data for the n^{th} frame and independently of the least significant bits of data (AAPA: pg. 7, par. [0012] – pg. 8, par. [0016]).

AAPA does not disclose expressly wherein the modulated most significant bits of data contain more data bits than do each of the most significant bits of data for the $(n-1)^{th}$ frame and the most significant bits of data for the n^{th} frame.

As can be seen from **Figure 4** of AAPA, a look-up table receives input most significant bit data and outputs modulated most significant bit data. HIROSAWA, analogous in art with AAPA, teaches/suggests a method of driving a liquid crystal display in **Figure 5** wherein input data of m-bits is received by a look-up table (**LUT**), the look-up table modulating the input data of m-bits by outputting modulated data of n-bits, wherein n is greater than m (n>m) (HIROSAWA: col. 5, ln. 20-30). This is accomplished by increasing the number of bits of the look-up table (HIROSAWA: col. 6, ln. 22-26).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of AAPA by increasing the number of bits of the look-up table such that the look-up table for receiving input data of m-bits outputs modulated data of n-bits, wherein n is greater than m, as taught/suggested by HIROSAWA. As a result, the modulated current most significant bit data containing more data bits than do each of the most significant bits of data of the $(n-1)^{th}$ and n^{th} frame.

The suggestion/motivation for doing so would have been to improve the precision of the data to be displayed (HIROSAWA: col. 6, ln. 22-26).

As to **Claims 2 and 6**, AAPA as modified by HIROSAWA above teaches/suggests wherein the current and delayed most significant bit data and the least significant bit data are 4 bits wide (AAPA: pg. 7, par. [0012] – pg. 8, par. [0016]), and the modulated current most significant bit data is m-bits wide, wherein m>4 (i.e. m>input) (HIROSAWA: col. 5, ln. 20-30).

Although neither AAPA nor HIROSAWA disclose expressly wherein the modulated current most significant bit data is 8-bits wide, the Examiner takes Official Notice that the utilization of data bit widths in powers of 2 (e.g. $2^1=2$, $2^2=4$, $2^3=8$, etc.) is old and well-known in the art.

Thus, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to further modify the teachings of AAPA and HIROSAWA such that the modulated current most significant bit data is 8 bits wide.

The suggestion/motivation for doing so would have been because computer-processing systems are known to operate with data bit widths in powers of 2.

As to **Claim 3**, AAPA teaches/suggests combining the current least significant bit data and the modulated current most significant bit data to generate an output video data (AAPA: pg. 7, par. [0012] – pg. 8, par. [0016]).

As to **Claim 4**, AAPA teaches/suggests wherein the generating modulated current most significant bit data comprises, selecting desirable data from a look-up table based on the current most significant bit data and the delayed most significant bit data; and outputting the selected data as the modulated current most significant bit data (AAPA: pg. 7, par. [0012] – pg. 8, par. [0016]).

As to **Claim 7**, AAPA teaches/suggests wherein the modulator includes a look-up table having available gray level values for the modulated most significant bits of data (AAPA: pg. 7, par. [0012] – pg. 8, par. [0016]).

As to **Claim 8**, AAPA teaches/suggests a liquid crystal display panel having a plurality of data lines and a plurality of gates lines; a data driver to combine the modulated most significant bits of data from the modulator and the least significant bits of data bypassed from the input line to generate a modulated video data and to supply the modulated video data to the data lines (AAPA: pg. 7, par. [0012] – pg. 8, par. [0016]); a gate driver to supply the scanning signals to the gate lines; and a timing controller to supply video data to the input line and to concurrently control the data driving and the gate driver, all of which are inherent in the driving of a liquid crystal display so as to selectively display frames of data.

As to **Claim 15**, AAPA teaches/suggests wherein the liquid crystal display comprises a liquid crystal display panel having a plurality of data lines, the method further comprising: driving the data lines with the output video data, all of which are inherent in the driving of a liquid crystal display so as to selectively display frames of data.

As to **Claims 16 and 18**, AAPA teaches/suggests wherein the look-up table stores available gray level values of the modulated current most significant bit data based on the available gray level values of the current most significant bit data and the available gray level values of the delayed most significant bit data (AAPA: pg. 7, par. [0012] – pg. 8, par. [0016]).

7. **Claims 1-11,15,16,18 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al. (U.S. Patent No. 6,943,763 B2, hereinafter SHIBATA) in view of Hirosawa et al. (U.S. Patent No. 5,123,059).

As to independent **Claim 1**, SHIBATA teaches/suggests a method of driving a liquid crystal display in **Figure 7**, comprising: dividing input data (**11**) into most significant bit data (**12,14**) and least significant bit data (**18**); delaying the most significant bit data (**12,13**) for one frame period; and generating modulated current most significant bit data (**15**) in accordance with a difference between the delayed most significant bit data (**13**) and the current most significant bit data (**14**) and independently from the least significant bit data (**18**) (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

SHIBATA does not disclose expressly wherein the modulated current most significant bit data contains more data bits than do each of the current most significant bit data and the delayed most significant bit data.

As can be seen from **Figure 7** of SHIBATA, a look-up table (**3**) receives input most significant bit data and outputs modulated most significant bit data. HIROSAWA, analogous in art with SHIBATA, teaches/suggests a method of driving a liquid crystal display in **Figure 5** wherein input data of m-bits is received by a look-up table (**LUT**), the look-up table modulating the input data of m-bits by outputting modulated data of n-bits, wherein n is greater than m (n>m) (HIROSAWA: col. 5, ln. 20-30). This is accomplished by increasing the number of bits of the look-up table (HIROSAWA: col. 6, ln. 22-26).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of SHIBATA by increasing the number of bits of the look-up table such that the look-up table for receiving input data of m-bits outputs modulated data of n-bits, wherein n is greater than m, as taught/suggested by HIROSAWA. As a result, the modulated current most significant bit data containing more data bits than do each of the most significant bits of data of the delayed and current frame.

The suggestion/motivation for doing so would have been to improve the precision of the data to be displayed (HIROSAWA: col. 6, ln. 22-26).

As to independent **Claim 5**, SHIBATA teaches/suggests a driving apparatus for a liquid crystal display in **Figure 7**, comprising: a memory (**2**) to receive most significant bits of data for an n^{th} frame from an input line (**12**) and to output the most significant bits of data for an $(n-1)^{th}$ frame (**13**); and a modulator (**3,7**) to modulate the most significant bits of data including most significant bits of data and least significant bits of the n^{th} frame (**14,18**) in accordance with a difference between the most significant bits of data for the $(n-1)^{th}$ frame (**13**) and the most significant bits of data for the n^{th} frame (**14**) and independently of the least significant bits of data (**18**) (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

SHIBATA does not disclose expressly wherein the modulated most significant bits of data contain more data bits than do each of the most significant bits of data for the $(n-1)^{th}$ frame and the most significant bits of data for the n^{th} frame.

As can be seen from **Figure 7** of SHIBATA, a look-up table receives input most significant bit data and outputs modulated most significant bit data. HIROSAWA, analogous in art with SHIBATA, teaches/suggests a method of driving a liquid crystal display in **Figure 5** wherein input data of m-bits is received by a look-up table (**LUT**), the look-up table modulating the input data of m-bits by outputting modulated data of n-bits, wherein n is greater than m (n>m) (HIROSAWA: col. 5, ln. 20-30). This is accomplished by increasing the number of bits of the look-up table (HIROSAWA: col. 6, ln. 22-26).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of SHIBATA by increasing the number of bits of the look-up table such that the look-up table for receiving input data of m-bits outputs modulated data of n-bits, wherein n is greater than m, as taught/suggested by HIROSAWA. As a result, the modulated current most significant bit data containing more data bits than do each of the most significant bits of data of the $(n-1)^{th}$ and n^{th} frame.

The suggestion/motivation for doing so would have been to improve the precision of the data to be displayed (HIROSAWA: col. 6, ln. 22-26).

As to independent **Claim 9**, SHIBATA teaches/suggests a liquid crystal display in **Figure 7**, comprising: a liquid crystal display panel (**6**) having a plurality of data lines and a plurality of gate lines thereon; a timing controller (**1**) to rearrange video data received from an input data (**11**) and outputting RGB data including most significant bits of the RGB data (**12,14**) and least significant bits of the RGB data (**18**) and first and second timing signals (**16,17**); a data modulator (**2,3**) to modulate the most significant bits of the RGB data (**12,13,14**) based on a look-up table (**3**) storing modulated most

significant bits of the RGB data, wherein the least significant bits of the RGB data (**18**) bypass the modulator (**2,3**); a data driver (**4,7**) to receive the first timing signal (**18**), and to combine the modulated most significant bits of the RGB data (**15**) and the least significant bits of the RGB data (**18**), which bypassed the data modulator (**2,3**), to generate a modulated video data (**19**), the data driver (**4,7**) supplying the modulated video data (**19**) to the liquid crystal display panel (**6**) through the data lines; and a gate driver (**5**) to receive the second timing signal (**17**) and to supply a scanning signal to the liquid crystal display panel (**6**) through the gate lines (SHIBATA: col. 6, ln. 62 – col. 7, ln. 5; col. 9, ln. 48 – col. 11, ln. 42).

SHIBATA does not disclose expressly wherein the modulated most significant bits of the RGB data contain more data bits than do the most significant bits of the RGB data.

As can be seen from **Figure 7** of SHIBATA, a look-up table (**3**) receives input most significant bit data and outputs modulated most significant bit data. HIROSAWA, analogous in art with SHIBATA, teaches/suggests a method of driving a liquid crystal display in **Figure 5** wherein input data of m-bits is received by a look-up table (**LUT**), the look-up table modulating the input data of m-bits by outputting modulated data of n-bits, wherein n is greater than m (n>m) (HIROSAWA: col. 5, ln. 20-30). This is accomplished by increasing the number of bits of the look-up table (HIROSAWA: col. 6, ln. 22-26).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of SHIBATA by increasing the number of bits of the look-up table such that the look-up table for receiving input data of m-bits outputs modulated data of n-bits, wherein n is greater than m, as taught/suggested by HIROSAWA. As a result, the modulated most significant bits of the RGB data contain more data bits than do the most significant bits of the RGB data.

The suggestion/motivation for doing so would have been to improve the precision of the data to be displayed (HIROSAWA: col. 6, ln. 22-26).

As to **Claims 2,6 and 11**, SHIBATA as modified by HIROSAWA above teaches/suggests wherein the current and delayed most significant bit data and the least significant bit data are 4 bits wide (SHIBATA: col. 6, ln. 8-25; col. 11, ln. 25-42), and the modulated current most significant bit data is m-bits wide, wherein m>4 (i.e. m>input) (HIROSAWA: col. 5, ln. 20-30).

Although neither SHIBATA nor HIROSAWA disclose expressly wherein the modulated current most significant bit data is 8-bits wide, the Examiner takes Official Notice that the utilization of data bit widths in powers of 2 (e.g. $2^1=2$, $2^2=4$, $2^3=8$, etc.) is old and well-known in the art.

Thus, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to further modify the teachings of SHIBATA and HIROSAWA such that the modulated current most significant bit data is 8 bits wide.

The suggestion/motivation for doing so would have been because computer-processing systems are known to operate with data bit widths in powers of 2.

As to **Claim 3**, SHIBATA teaches/suggests combining the current least significant bit data (**18**) and the modulated current most significant bit data (**15**) to generate an output video data (**19**) (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

As to **Claim 4**, SHIBATA teaches/suggests wherein the generating modulated current most significant bit data (**15**) comprises, selecting desirable data from a look-up table based on the current most significant bit data (**14**) and the delayed most significant bit data (**13**); and outputting the selected data as the modulated current most significant bit data (**15**) (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

As to **Claim 7**, SHIBATA teaches/suggests wherein the modulator (**3**) includes a look-up table (**3**) having available gray level values for the modulated most significant bits of data (**15**) (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

As to **Claim 8**, SHIBATA teaches/suggests a liquid crystal display panel (**6**) having a plurality of data lines and a plurality of gates lines; a data driver (**4,7**) to combine the modulated most significant bits of data (**15**) from the modulator (**3**) and the least significant bits of data (**18**) bypassed from the input line to generate a modulated video data (**19**) and to supply the modulated video data (**19**) to the data lines; a gate driver (**5**) to supply the scanning signals to the gate lines; and a timing controller (**1**) to supply video data to the input line and to concurrently control the data driving and the gate driver (**5**) (SHIBATA: col. 6, ln. 62 – col. 7, ln. 5; col. 9, ln. 48 – col. 11, ln. 42).

As to **Claim 10**, SHIBATA teaches/suggests wherein the data modulator (**2,3**) includes: a frame memory (**2**) delaying current most significant bits of the RGB data (**12**) for one frame period and outputting the delayed most significant bits of the RGB data (**13**); and a look-up table (**3**) receiving both the current most significant bits of the RGB data (**14**) and the delayed most significant bits of the RGB data (**13**) and outputting the modulated most significant bits of the RGB data (**15**) (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

As to **Claim 15**, SHIBATA teaches/suggests wherein the liquid crystal display comprises a liquid crystal display panel having a plurality of data lines, the method further comprising: driving the data lines with the output video data (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

As to **Claims 16 and 18**, SHIBATA teaches/suggests wherein the look-up table (**3**) stores available gray level values of the modulated current most significant bit data (**15**) based on the available gray level values of the current most significant bit data (**14**) and the available gray level values of the delayed most significant bit data (**13**) (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

As to **Claim 20**, SHIBATA teaches/suggests wherein the look-up table (**3**) stores available gray level values of the modulated most significant bits of the RGB data (**15**) based on the available gray level values of the current most significant bits of the RGB data (**14**) and the available gray level values of the delayed most significant bits of the RGB data (**13**) (SHIBATA: col. 9, ln. 48 – col. 11, ln. 42).

Conclusion

8. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Alexander S. Beck** whose telephone number is **(571) 272-7765**. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Sumati Lefkowitz** can be reached on **(571) 272-3638**. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

asb
1/20/07

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER